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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,178	03/17/2004	Yasunori Kurosawa	81754.0114	4143

26021 7590 05/16/2006

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,178	KUROSAWA ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8 and 10-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-8 and 10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claims 2-8 and 10-14 is withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

The cancellation of claims 1, 9 and 15-20 in paper filed on 05/01/06 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-6 and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narizuka et al. (6,756,688) in view of Hsuan et al. (U.S. Pat. 6,166,444).

Regarding claims 2 and 10, Narizuka (Fig. 3e) discloses a semiconductor device, comprising: a semiconductor chip 11 and pad 12 (column 6, lines 1-3); a wiring layer 13 that has a concave portion (see Fig. 3e labeled by the examiner below) and is electrically connected to the pad 12; an external terminal 17 that is joined to the concave portion of the wiring layer 13; and a polyimide or epoxy resin layer 16 (column 8, line 23) provided with a through hole and disposed on the wiring layer 13, the through

hole and the concave portion residing at the same position, wherein a width of the concave portion increase with a depth of the concave portion (see Fig. 3e below).

Narizuka discloses a semiconductor chip 11 and a pad 12, but does not specifically disclose that the semiconductor chip 11 provided with an integrated circuit and the pad 12 is electrically connected to the integrated circuit.

However, Hsuan (Fig. 3) teaches a semiconductor chip 30 provided with an integrated circuit 32 and a pad 42 (column 3, lines 19-20), the pad 42 is electrically connected to the integrated circuit 32 (column 3, lines 15-17) and to the external terminals 56. Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide the semiconductor chip of Narizuka with the pad 54 electrically connected to the integrated circuit in order to provide the electrically connects between the integrated circuit and the external terminals, as taught by Hsuan (see Fig. 3).

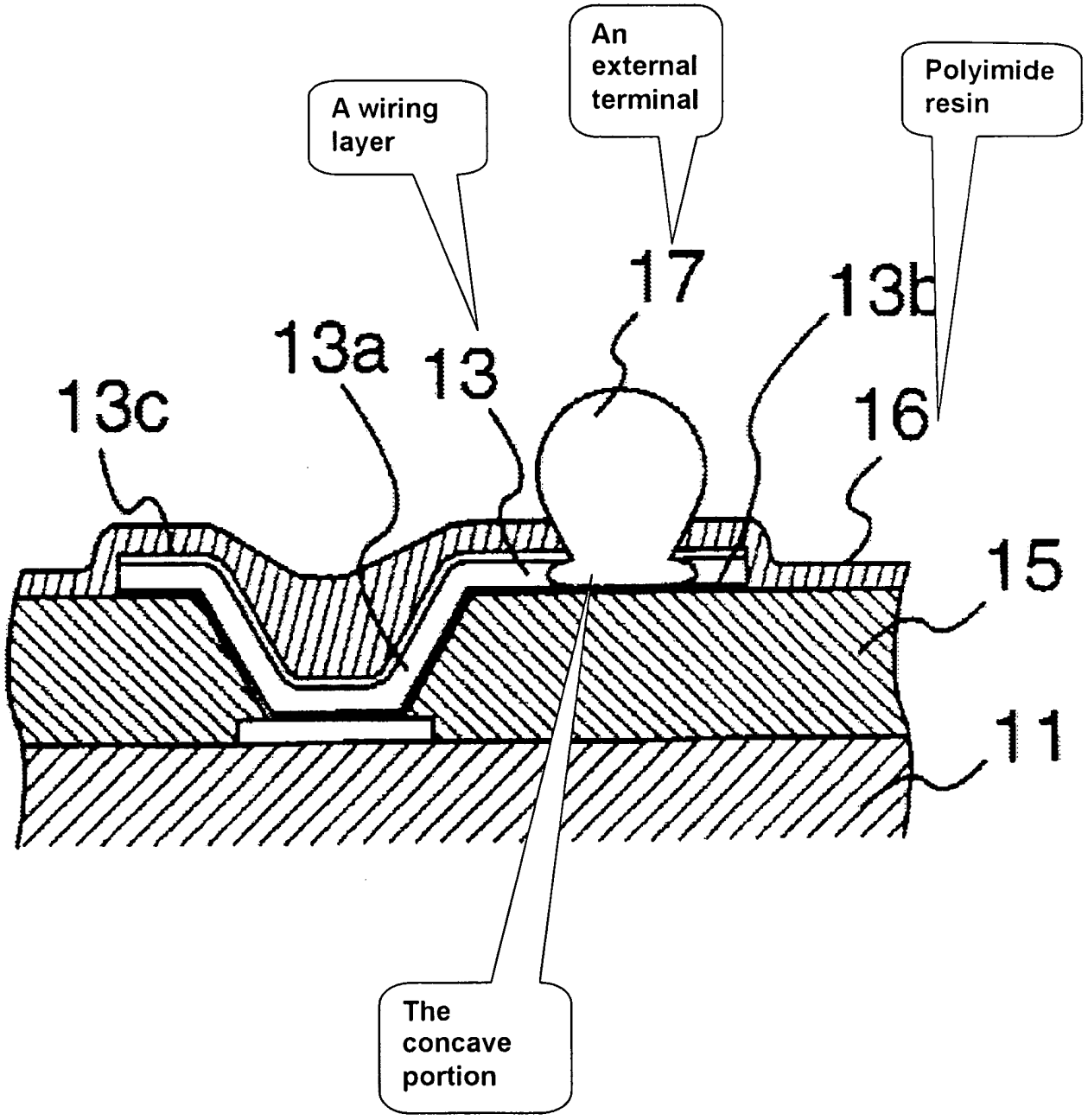
A wiring layer
An external terminal
Polyimide resin
17
13b
13a
13
13c
16
15
11
The concave portion

FIG. 3(e)

Regarding claims 3 and 11, Narizuka (Fig. 3e) discloses a semiconductor device, comprising: a semiconductor chip 11 and pad 12 (column 6, lines 1-3); a wiring layer 13 that has a concave portion (see Fig. 3e labeled by the examiner above) and is electrically connected to the pad 12; an external terminal 17 that is joined to the concave portion of the wiring layer 13; and a polyimide or epoxy resin layer 16 (column 8, line 23) provided with a through hole and disposed on the wiring layer 13, the through hole and the concave portion residing at the same position, wherein the concave portion has a first width at a first depth and a second width at a second depth that is deeper than the first depth, the first width being larger than an opening size of the concave portion and the second width being smaller than the first width (see Fig. 3e below).

Narizuka discloses a semiconductor chip 11 and a pad 12, but does not specifically disclose that the semiconductor chip 11 provided with an integrated circuit and the pad 12 is electrically connected to the integrated circuit.

However, Hsuan (Fig. 3) teaches a semiconductor chip 30 provided with an integrated circuit 32 and a pad 42 (column 3, lines 19-20), the pad 42 is electrically connected to the integrated circuit 32 (column 3, lines 15-17) and to the external terminals 56. Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide the semiconductor chip of Narizuka with the pad 54 electrically connected to the integrated circuit in order to provide the electrically connects between the integrated circuit and the external terminals, as taught by Hsuan (see Fig. 3).

Regarding claims 4 and 12, Narizuka discloses that an inner surface of the through hole in the resin layer 16 is in contact with the external terminal 17 (see Fig. 3e Labeled by the examiner above).

Regarding claims 5 and 13, Narizuka further discloses a stress relaxation layer 15 (column 6, lines 4-5) disposed on the semiconductor chip 11, wherein the wiring layer 13 is disposed on the stress relaxation layer 15.

Regarding claims 6 and 14, Narizuka discloses that the resin layer 16 is prepared from a solder resist of polyimide.

4. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narizuka et al. (6,756,688) in view of Hsuan et al. (U.S. Pat. 6,166,444) as applied to claim 2 above, and further in view of Farnworth et al. (U.S. Pat. 6,767,817) as previously cited.

Regarding claim 7, Narizuka does not disclose that a circuit board comprising the semiconductor chip 11 disclosed in Fig. 3e.

However, Farnworth (Fig. 2) teaches an integrated circuit package 36 (column 4, lines 1-3) including a circuit board 54 comprising a semiconductor chip 40 (column 4, lines 14-17). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide a circuit board comprising the semiconductor chip 11 of Narizuka in order to form an integrated circuit package which

is used in the desired electronic applications, as taught by Farnworth (column 4, lines 1-5).

Regarding claim 8, Narizuka does not disclose that an electronic apparatus comprising the semiconductor chip 11 disclosed in Fig. 3e.

However, Farnworth (Fig. 1) also teaches an electronic apparatus system 10 comprising an integrated circuit package 36 including a semiconductor chip 40 (Fig. 2 and column 4, lines 1-5). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide an electronic apparatus comprising the semiconductor chip 11 of Narizuka in order to form a desired electronic application such as a computer, audio or visual device, as taught by Farnworth (column 3, lines 15-21).

Conclusion

5. This action is made non-final.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
May 11, 2006.